

PHONE: 303 554-8371 FAX: 303 554-8667

Facsimile

Date: November 12, 2003
Deliver To: Examiner Zarneke (Art Unit 2827)
Fax: 703-746-3876
Re: 10/059,686
From: David M. Sigmond

~~TECHNOLOGY CENTER 2003~~

~~FAX RECEIVED~~

~~NOV 3 1 2003~~

~~TECHNOLOGY CENTER 2003~~

Copies of the following documents are attached:

1. Response filed April 25, 2003 (25 pages)
2. Return Postcard establishing PTO receipt of Response

Please let me know if I can assist further.

~~FAX RECEIVED~~
~~NOV 1 3 2003~~
~~TECHNOLOGY CENTER 2003~~

TOTAL NUMBER OF PAGES: 27 (Including This Page)
*If you have any trouble receiving this transmission, please call
David M. Sigmond at (303) 554-8371*

SPECIAL INSTRUCTIONS:

The documents accompanying this facsimile transmittal coversheet contain information from David M. Sigmond which may be confidential and/or legally privileged and are valuable, and proprietary to, trade secrets of, and copyrighted by David M. Sigmond or his clients. The documents are intended only for the personal and confidential use of the addressee identified above. If you are not the intended recipient or an agent responsible for delivering these documents to the intended recipient, you are hereby notified that any review, disclosure, copying, distribution or the taking of any action in reliance on the contents of this transmitted information is strictly prohibited.

IF YOU HAVE RECEIVED THIS FACSIMILE IN ERROR, PLEASE IMMEDIATELY NOTIFY DAVID M. SIGMOND SO THAT I CAN ARRANGE FOR THE RETURN OF THE ORIGINAL DOCUMENTS TO ME OR TO THE INTENDED RECIPIENT. THANK YOU.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Cheng-Lien Chiang
Assignee: Bridge Semiconductor Corporation
Title: METHOD OF MAKING A SEMICONDUCTOR PACKAGE
DEVICE THAT INCLUDES A CONDUCTIVE TRACE WITH
RECESSED AND NON-RECESSED PORTIONS
Serial No.: 10/059,686 Filed: January 29, 2002
Examiner: Zarneke, D. Group Art Unit: 2827
Atty. Docket No.: BDG005-1

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

RESPONSE

In response to the Office Action dated April 18, 2003, please amend the application as follows.

In the Title

The Title has been replaced with:

METHOD OF MAKING A SEMICONDUCTOR PACKAGE DEVICE THAT INCLUDES A
CONDUCTIVE TRACE WITH RECESSED AND NON-RECESSED PORTIONS

In the Specification

Replace the paragraph at page 10, lines 5-14 with the following paragraph:

FIGS. 1A and 1B are top and bottom perspective views, respectively, of semiconductor chip 110 which is an integrated circuit in which various transistors, circuits, interconnect lines and the like are formed (not shown). Chip 110 includes opposing major surfaces 112 and 114